ABSTRACT OF THE DISCLOSURE

An UART receives asynchronous transmission serial data based on a baud-rate clock from a DTE. An MPU analyzes the data received by the UART. A baud-rate generating portion generates the baud-rate clock to be output to the UART in accordance with instructions from the MPU. A first counter measures the span of the start bit of the first character of an AT command transmitted from the DTE based on instructions from the MPU. A decoder receives a measurement result of the first counter, outputs frequency-dividing data for producing a clock for sampling the first character, and also outputs, when the rate of the start bit is more than a preset value, a flag indicating this matter. A second counter selects, in accordance with whether or not the flag is has been set, the frequency-dividing data from either the decoder or the MPU, and produces the sampling clock. A shift register receives data subsequent to the start bit of the first character based on the sampling clock from the second register, holds the received data, which data is then read by the MPU.